When programming is made at these timings, drain disturb can be restricted because the drain voltage application time is short.

It is also possible to apply +3.3 V to the selected word line WLn at the timing t0 and +1 V to the diffusion layer Dn at the timing t1 (t0 < t1) as shown in Fig. 21C. Next, +3.3 V is applied to the third gate AGe at the timing t2 (t1 < t2). This voltage is kept for a predetermined read time t (t = t3 - t2), and the voltage of the third gate AGe is returned to 0 V at the timing t3. The voltage of the diffusion layer Dn is returned to 0 V at the timing t4 (t3 < t4), and the voltage of the selected word line WLn is returned to 0 V at the timing t4 (t3 < t4). Alternatively, it is possible to apply +1 V to the diffusion layer Dn at the timing t0 and +3.3 V to the selected word line WLn at the timing t1 (t0 < t1). Next, +3.3 V is applied to the third gate AGe at the timing t2 (t1 < t2). This voltage is kept for a predetermined read time t (t = t3 - t2) and the voltage of the third gate AGe is returned to 0 V at the timing t3. The voltage of the selected word line is returned to 0 V at the timing t4 (t3 < t4), and the voltage of the diffusion layer is returned to 0 V at the timing t5 (t4 < t5).

As shown in Fig. 21F, +1 V is applied to the diffusion layer Dn at the timing t0, and +3.3 V is applied to the third gate AGe at the timing t1 (t0 < t1). Next, +3.3 V is applied to the selected word line WLn at the timing t2 (t1 < t3). This voltage is kept for a

When programming is made at these timings, drain disturb can be restricted because the drain voltage application time is short.

It is also possible to apply +3.3 V to the selected word line WLn at the timing t0 and +1 V to the diffusion layer Dn at the timing t1 (t0 < t1) as shown in Fig. 21C. Next, +3.3 V is applied to the third gate AGe at the timing t2 (t1 < t2). This voltage is kept for a predetermined read time t (t = t3 - t2), and the voltage of the third gate AGe is returned to 0 V at the timing t3. The voltage of the diffusion layer Dn is returned to 0 V at the timing t4 (t3 < t4), and the voltage of the selected word line WLn is returned to 0 V at the timing t4 (t3 < t4). Alternatively, it is possible to apply +1 V to the diffusion layer Dn at the timing t0 and +3.3 V to the selected word line WLn at the timing t1 (t0 < t1). Next, +3.3 V is applied to the third gate AGe at the timing t2 (t1 < t2). This voltage is kept for a predetermined read time t (t = t3 - t2) and the voltage of the third gate AGe is returned to 0 V at the timing t3. The voltage of the selected word line is returned to 0 V at the timing t4 (t3 < t4), and the voltage of the diffusion layer is returned to 0 V at the timing t5 (t4 < t5).

As shown in Fig. 21F, +1 V is applied to the diffusion layer Dn at the timing t0, and +3.3 V is applied to the third gate AGe at the timing t1 (t0 < t1). Next, +3.3 V is applied to the selected word line WLn at the timing t2 (t1 < t3). This voltage is kept for a